09-20-00 A

NEW, CONTINUATION, DIVISIONAL OR CONTINUATION-IN-PART APPLICATION UNDER 37 C.F.R. §1.53(b)

Attorney Docket No. 9319S-000157

Express Mail Label No. EL581391736US

Date September 19, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Hon. Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R §1.53(b) is a patent application for: Conductor-Pattern Testing Method, and Electro-Optical Device

identified by: [ ] First named inventor: Koichi Miyasaka
or [X] Attorney Docket No. (see above)

1. **Type of Application**

[X] This application is a new (non-continuing) application.

[ ] This application is a [ ] continuation / [ ] divisional / [ ] continuation-in-part of prior application No. ____. Amend the specification by inserting before the first line the sentence:

--This is a [continuation/division/continuation-in-part] of United States patent application No. ____, filed ____.--

[ ] The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

If for some reason applicant has not requested a sufficient extension of time in the parent application, and/or has not paid a sufficient fee for any necessary response in the parent application and/or for the extension of time necessary to prevent the abandonment of the parent application prior to the filing of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 08-0750 for any fee that may be due. THIS FORM IS BEING FILED IN TRIPLICATE: one copy for this application; one copy for use in connection with the Deposit Account (if applicable); and one copy for the above-mentioned parent application (if any extension of time is necessary).

2. **Contents of Application**

a. [X] Specification of 25 pages;
[ ] A microfiche computer program (Appendix);
[ ] A nucleotide and/or amino acid sequence submission;

[ ] Because the enclosed application is in a non-English language, a verified English translation [ ] is enclosed [ ] will be filed.

[ ] Cancel original claims ____ of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing date purposes.)

b. [X] Drawings on 5 sheets;

c. [X] A signed Oath/Declaration [ ] is enclosed / [X] will be filed in accordance with 37 C.F.R. §1.53(f).

The enclosed Oath/Declaration is [ ] newly executed / [ ] a copy from a prior application under 37 C.F.R. §1.63(d) / [ ] accompanied by a statement requesting the deletion of person(s) not inventors in the continuing application.

d. **Fees**

FILING FEE CALCULATION	Number Filed		Number Extra		Rate		Basic Fee $690.00
Total Claims	9	- 20 =	0	×	$18.00	=	0
Independent Claims	3	- 3 =	0	×	$78.00	=	0
Multiple Dependent Claim(s) Used					$260.00	=	
FILING FEE - NON-SMALL ENTITY							690.00
FILING FEE - SMALL ENTITY: Reduction by 1/2 [ ] Verified Statement under 37 C.F.R. §1.27 is enclosed. [ ] Verified Statement filed in prior application.							
Assignment Recordal Fee ($40.00)							
37 C.F.R. §1.17(k) Fee (non-English application)							
TOTAL							**690.00**

[ ] A check is enclosed to cover the calculated fees. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to Deposit Account No. 08-0750. A duplicate copy of this document is enclosed.

[X] The calculated fees will be paid within the time allotted for completion of the filing requirements.

[ ] The calculated fees are to be charged to Deposit Account No. 08-0750. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to said Deposit Account. A duplicate copy of this document is enclosed.

3. **Priority Information**

[X] **Foreign Priority**: Priority based on Japanese Application No. 11-266002 filed September 20, 1999, is claimed.

[X] A copy of the above referenced priority document [X] is enclosed / [ ] will be filed in due course, pursuant to 35 U.S.C. §119(a)-(d).

[ ] **Provisional Application Priority**: Priority based on United States Provisional Application No. ____, filed ____, is claimed under 35 U.S.C. §119(e).

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4. **Other Submissions**

[ ] A Preliminary Amendment is enclosed.

[X] An Information Disclosure Statement, 1 sheets of PTO Form 1449, and 1 patent(s)/publications/documents are enclosed.

[ ] A power of attorney

[ ] is submitted [ ] with the new Oath/Declaration.

[ ] is of record in the prior application and [ ] is in the original papers / [ ] a copy is enclosed.

[ ] An Assignment of the invention

[ ] is enclosed with a cover sheet pursuant to 37 C.F.R. §§3.11, 3.28 and 3.31.

[ ] is of record in a prior application. The assignment is to ____, and is recorded at Reel ____, Frame(s) ____.

[ ] An Establishment of Assignee's Right To Prosecute Application Under 37 C.F.R. §3.73(b), and Power Of Attorney is enclosed.

[X] An Express Mailing Certificate is enclosed.

[ ] Other: _____

_____

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Respectfully,

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EXPRESS MAILING CERTIFICATE

Applicant:	Koichi Miyasaka
Serial No. (if any):	Not Yet Assigned
Filed:	Herewith
For:	Conductor-Pattern Testing Method, and Electro-Optical Device
Docket:	9319S-000157
Attorney:	GGS/BEW

"Express Mail" Mailing Label Number EL581391736US

Date of Deposit..... September 19, 2000

I hereby certify and verify that the accompanying Transmittal letter (in duplicate), 25 page Patent Application, 5 sheets of informal drawings showing Figures 1-8, Information Disclosure Statement, Form PTO 1449, copies of the references cited therein (1JP), certified copy of the priority document (JP 11-266002, filed 9/20/99), this certificate, and an acknowledgement postcard are being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is (are) addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Michele S. Mester

Signature of Person Mailing Document(s)

CONDUCTOR-PATTERN TESTING METHOD, AND ELECTRO-OPTICAL DEVICE

BACKGROUND

1. Technical Field of the Invention

The present invention relates to a method of inspecting a conductor pattern as well as to electro-optical devices, and more specifically to a pattern structure which can be suitably implemented as an electrode pattern or a wiring pattern formed on a substrate constituting a liquid crystal panel and to a method of inspecting such a pattern.

2. Description of the Related Art

A typical liquid crystal device is formed by a pair of transparent substrates attached together via a sealant, with liquid crystals filled in the space between the two substrates and surrounded by the sealant, i.e., a liquid crystal sealed area.

An example of liquid crystal device construction is shown in Fig. 4 and Fig. 5. Fig. 4 is a perspective plan view which schematically illustrates the planar structure of a liquid crystal device 10, while Fig. 5 is an expanded sectional view schematically showing the structure of the liquid crystal device 10 in the vicinity of an extended area 11s. The liquid crystal device 10 is defined by a pair of transparent substrates 11 and 12 attached together via a sealant 13, wherein the transparent substrate 11 is made

somewhat wider than the transparent substrate 12 so as to have an extended area 11s projecting horizontally beyond one end of the transparent substrate 12. The rectangular interior of the sealant 13 constitutes a liquid crystal sealed area A.

Inside the liquid crystal sealed area A, transparent electrodes 11a are formed on the transparent substrate 11. The transparent electrodes 11a passes beneath the sealant 13 and is pulled onto the surface of the extended area 11s to form wiring lines 11b. Within the scope of the liquid crystal sealed area A, an overcoat film 15 is formed over the transparent electrodes 11a, and an alignment film 16 is further formed over the overcoat film 15. Meanwhile, transparent electrodes 12a are formed on the transparent substrate 12. The transparent electrodes 12a extend in the direction orthogonal to the transparent electrodes 11a, and then leads up to where the sealant 13 is formed. On the transparent electrodes 12a, an alignment film 17 is formed. In between the alignment films 16 and 17, liquid crystals (not shown) are filled, which will be aligned in accordance with the surface conditions of the alignment films 16 and 17.

On the extended area 11s, wiring lines 11c are formed on both sides of the wiring lines 11b in a particular pattern. The wiring lines 11c extends on the transparent

substrate 11 up to where the sealant 13 is formed. The sealant 13 is made of resin materials containing conductive particles, and exhibits anisotropic conductivity, i.e., is made electrically conductive only in the depth direction (gap direction) of the substrates, by being pressurized between the transparent substrate 11 and the transparent substrate 12. The transparent electrodes 12a and the wiring lines 11c vertically overlap at a vertically-conductive crossover 13b of the sealant 13, and thus are electrically connected via the vertically-conductive crossover 13b.

The wiring lines 11b and 11c are electrically connected via an anisotropic conductive film 8 to the output terminals (not shown) of the driver IC 18 for driving the liquid crystal device 10. On the extended area 11s, a terminal pattern 11d is also formed. One end of the terminal pattern 11d is electrically connected to the input terminals of the driver IC 18 via an anisotropic conductive film 8, while the other end of the terminal pattern 11d is electrically connected to wiring members 9 of a flexible wiring board, a tape automated bonding (TAB) substrate, etc..

The wiring lines 11b and 11c on the extended area 11s are formed with a small line width and in a fine pitch, and hence are vulnerable to dust and acids and also involves the danger of galvanic corrosion. Thus, after mounting the driver IC 18 and the wiring members 9, the overall mounting

plane of the extended area 11s is covered with resin mold 19 containing silicone resin or the like.

In the liquid crystal sealed area A, the transparent electrodes 11a and the transparent electrodes 12a are arranged in a matrix to form a display driving area E. The display driving area E allows to display particular images in accordance with the potentials supplied to each of the transparent electrodes 11a and transparent electrodes 12a. The liquid crystal sealed area A also includes a non-driving area F (non-active area) surrounding the display driving area E (active area). In the non-driving area F, dummy conductors 11f are formed to constitute a dummy pattern 11F. Fig. 6 is an expanded plan view showing a part of the display driving area E and the non-driving area F. The non-driving area F essentially need not be provided with electrodes for driving the liquid crystal device. In the absence of the electrodes, however, the non-driving area F would have a thicker liquid crystal sealed area than that of the display driving area E, and the orientation of the liquid crystals would be altered, resulting in a different appearance from that of the display driving area E. Accordingly, as mentioned above, a dummy pattern 11 F is formed which are provided with a plurality of dummy conductors 11f, such as dummy electrodes and dummy wiring lines, having no external connections. The dummy conductors

11f are formed at the same time and with the same material as the transparent electrodes 11a, the wiring lines 11b and the wiring lines 11c.

During the manufacturing process of a liquid crystal device as described above, after the transparent electrodes 11a, wiring lines 11b and 11c are formed on the transparent substrate 11, a pattern inspection may be performed to ensure that no short circuit occurs between any of the electrodes or wiring lines. In a typical pattern inspection, as shown in Fig. 6, a pair of probes 3a and 3b are simultaneously made to contact respectively on one of two mutually-adjacent transparent electrodes 11a to check whether there occurs a short circuit between the two transparent electrodes 11a. The inspection is performed for each set of two adjacent transparent electrodes 11a by progressively moving the probes 3a and 3b to the next respective transparent electrodes 11a one by one in the array direction of the transparent electrodes (right-and-left direction as viewed in Fig. 6). If a short circuit is observed between any of the transparent electrodes 11a, either the short-circuited part is repaired, or the transparent substrate 11 is abandoned as defective.

In the inspection process, the relative position of the pair of probes 3a and 3b is so prescribed that the probes 3a and 3b are spaced in the array direction of the transparent

electrodes 11a (left-and-right direction as viewed in Fig. 6) by an amount equivalent to the pattern pitch of the transparent electrodes 11a in order to ensure that each of the probes 3a and 3b will contact respectively on one of two adjacent transparent electrodes 11a. Further, the probes 3a and 3b are so arranged to have a relative deviation in the extending direction of the transparent electrodes 11a (top-and-bottom direction as viewed in Fig. 6) in order to ensure a sufficient interval between the probes 3a and 3b, which serves to prevent short-circuiting between the probes 3a and 3b per se and to facilitate fixing of the probes.

In a conventional inspection process as described above which progressively inspects each set of two adjacent transparent electrodes 11a, a tester 3 having the probes 3a and 3b, as shown in Fig. 8, while maintaining a fixed interval between the probes 3a and 3b, performs progressive scanning in the array direction of the transparent electrodes 11a (right-and-left direction as viewed in Fig. 8) by having each of the probes 3a and 3b contact respectively on one of two adjacent transparent electrodes 11a in a repetition by the pitch of the transparent electrodes 11a. The dummy pattern 11F, if formed in the array direction of the transparent electrodes 11a (to the right as viewed in Fig. 8) is typically constituted by dummy conductors 11f which are wider than the transparent

electrodes 11a and rather long in shape. This causes the probes 3a and 3b to contact simultaneously on a single dummy conductor 11f to get short-circuited. Thus, a short circuit is detected because of the dummy conductor 11f even if the non-dummy transparent electrodes 11a are non-defective. Fig. 7 is a graph illustrating a progress of a conventional inspection of an electrode pattern or a wiring pattern. On encountering dummy conductors 11f during the inspection process as described above, the probes 3a and 3b get short-circuited. Then the tester 3 detects an abnormal test result as at W in Fig. 7, thereby erroneously determining that there exists a pattern defect. It may be figured out that the non-dummy transparent electrodes 11a are actually non-defective, but only through a laborious work of analyzing test results for each substrate pattern.

Accordingly, in order to overcome the above-described problem, it is an object of the present invention to provide a method as well as a structure which prevents erroneous detection resulting from a dummy pattern in an inspection of a conductor pattern.

SUMMARY OF THE INVENTION

To overcome the foregoing problem, the present invention provides a conductor-pattern testing method for inspecting an electrode substrate having a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each other on a base and further having a dummy pattern constituted by a plurality of dummy conductors formed in an area on the base where the conductor pattern is not formed, the method examining electrical characteristics among the plurality of conductors by establishing the contact of at least two probes having a positional relationship defined so that the two probes are brought into contact with at least two conductors among the plurality of conductors, wherein the plurality of dummy conductors disposed in the array direction of the plurality of conductors to constitute the dummy pattern are formed in segments so as to prevent two or more of the probes from being simultaneously in contact with any one of the plurality of dummy conductors and the at least two probes are progressively moved for inspection in the array direction of the plurality of conductors.

According to the present invention, dummy conductors disposed in the array direction of the plurality of conductors are formed in segments, and two or more among the probes are prevented from being simultaneously in contact

with the same dummy conductor. Thus, short-circuiting between probes, caused by the dummy conductors, does not occurs even when the at least two probes are progressively moved for inspection in the array direction of the plurality of conductors. This can prevent false determination, and can detect rapid and easy detection of a defect in the conductor pattern from the determination result.

In the present invention, the conductors are preferably electrodes or wiring lines formed on the base.

The present invention serves to readily detect defects including short-circuiting between the electrodes or wiring lines formed on the base.

In the present invention, it is preferable that the dummy conductors disposed in the array direction of the electrodes to constitute the dummy pattern are mutually set apart between any pair of the probes in the extending direction of the electrodes.

According to the present invention, by forming the dummy conductors so as to be set apart between any pair of probes in the extending direction of the conductors, short circuits between the probes are readily prevented while not making the dummy pattern too complex. When the dummy conductors are separated in the extending direction particularly be spacing lines (pattern gaps) extending in the array direction of the conductors, providing spacing

lines in the number corresponding to the number of probe intervals will suffice to prevent short circuiting between the probes. It is to be noted that, in this application, being separated in the direction X indicates being separated so that there shall be no electrical conductivity in the direction X.

In the present invention, each of the dummy conductors disposed in the array direction of the conductors to constitute the dummy pattern is preferably shorter when viewed along the extending direction of the conductors than the minimum length between any pair of the probes in the extending direction of the conductors.

According to the present invention, by forming the dummy conductors so as to be shorter when viewed along the extending direction of the conductors than the minimum length between any pair of the probes in the extending direction of the conductors, short circuits between the probes do not occur even if the testing positions of a plurality of the probes are deviated in the extending direction of the conductors, and thus erroneous detection resulting from the dummy pattern may be prevented more adequately.

In the present invention, the dummy conductors disposed in the array direction of the conductors to constitute the dummy pattern are mutually separated in the array direction

of the conductors in a pitch equivalent to the array pitch of the conductors.

According to the present invention, by separating the dummy conductors in the array direction of the conductors in a pitch equivalent to the array pitch of the conductors, each of the probes, intended to contact respectively on distinct one of conductors, will contact respectively on distinct one of dummy conductors, preventing short circuits between the probes. It is further preferable to form the conductors and the dummy conductors so as to be in phase with each other. This ensures that each of the probes will respectively contact on distinct one of dummy conductors without altering the operation cycle of the probes, thereby further ensuring prevention of short circuits between the probes.

Preferably in the present invention, the base is a substrate, and the electrode substrate is an electro-optical device in which a plurality of electrodes and wiring lines are formed in a particular pattern on the surface of the substrate and electro-optical material to be affected by an electric field generated by the electrodes are further disposed thereover.

An electro-optical device according to the present invention includes: a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each

other on a base; a dummy pattern, which are not required to work as the conductors, constituted by a plurality of dummy conductors formed in an area on the base where the conductor pattern is not formed; and electro-optical material disposed on the conductor pattern. In the electro-optical device, the dummy conductors disposed in the array direction of the conductors to constitute the dummy pattern are mutually separated in the extending direction of the conductors. Each of the dummy conductors is preferably shorter when viewed along the extending direction of the conductors than the minimum length between any pair of the probes in the extending direction of the conductors. Thus, erroneous detection resulting from the dummy pattern may be prevented by forming each of the dummy conductors to be shorter than a certain length when viewed along the extending direction of the conductors and performing inspections with a probe interval not less than the particular length.

Another electro-optical device according to the present invention includes: a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each other on a base; a dummy pattern, which are not required to work as the conductors, constituted by a plurality of dummy conductors formed in an area on the base where the conductor pattern is not formed; and electro-optical material disposed on the conductor pattern. In the electro-optical device,

the dummy conductors disposed in the array direction of the conductors to constitute the dummy pattern are mutually separated in the array direction of the plurality of conductors in a pitch substantially equivalent to the array pitch of the conductors.

In the electro-optical device, it is preferable that the plurality of dummy conductors disposed in the array direction of the conductors to constitute the dummy pattern are mutually separated in the extending direction of the conductors.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an expanded plan view showing a liquid crystal device, which operates the inspection method of a conductor pattern, in the vicinity of an extended area according to the present invention.

Fig. 2 is a schematic diagram illustrating a method of inspecting a conductor pattern as well as a dummy pattern structure according to the present invention.

Fig. 3 is a schematic diagram illustrating a method of inspecting a conductor pattern as well as another dummy pattern structure according to the present invention.

Fig. 4 is a perspective plan view of the overall structure of a liquid crystal device.

Fig. 5 is an expanded sectional view showing the structure of a liquid crystal device in the vicinity of an extended area.

Fig. 6 is a schematic diagram illustrating a method of inspecting an electrode pattern on a substrate constituting a conventional liquid crystal device.

Fig. 7 is a graph schematically showing a test result obtained by a conventional inspection method.

Fig. 8 is a schematic illustration of a conventional inspection method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A method of inspecting a conductor pattern as well as an electro-optical device according to the present invention will now be described in detail in their preferred embodiments. It is to be noted that, although the embodiments described below are concerned with a method of inspecting an electrode pattern or a wiring pattern formed on a substrate (panel substrate) constituting a liquid crystal device (liquid crystal panel) as well as a construction of such a liquid crystal device, the present invention is applicable to a variety of conductor patterns not only to an electrode pattern or a wiring pattern on a substrate constituting a liquid crystal device, but also to

a variety of electro-optical devices including luminescence devices or plasma display devices as well as liquid crystal devices.

Fig. 1 is a fragmentary expanded plan view showing a part of a transparent substrate 11 constituting a liquid crystal device according to a preferred embodiment. The liquid crystal device of this embodiment is constructed as identical to the liquid crystal device 10 shown in Fig. 4 and Fig. 5, except for the pattern structure of transparent conductors formed on the transparent substrate 11.So the description as to the identical construction will be omitted.

Referring to Fig. 1, on the surface of the transparent substrate 11, there are provided: transparent electrodes 11a, wiring lines 11b and 11c, a terminal pattern 11d, formed by depositing, for example, indium tin oxide (ITO) by the sputtering method; and a dummy pattern 11G formed in the non-driving area F outside the display driving area E where the transparent electrodes 11a are formed. On the dummy pattern 11G, there are formed a multiplicity of dummy conductors 11g. As is conventional, these dummy conductors are so arranged as to extend substantially over the entire non-driving area F.

In this embodiment, the dummy pattern 11G is so configured that the dummy conductors 11g are mutually set

apart with spacing therebetween as appropriate in the extending direction (top-and-bottom direction as viewed in Fig. 1) and in the array direction (right-and-left direction as viewed in Fig. 1) of the transparent electrodes 11a. In the example illustrated in Fig. 1, a dummy pattern 11G, which substantially extends over the entire non-driving area F, includes on both sides in the array direction of the transparent electrodes 11a (to the right and to the left in Fig. 1): dummy conductors 11g(1) whose width and spacing are so arranged that the transparent electrodes 11a and the dummy conductors 11g(1) are formed in a substantially equivalent pitch in the array direction; and dummy conductors 11g(2), whose pitch in the array direction is different from that of the transparent electrodes 11a, yet each of which are mutually separated so as to be shorter than a prescribed interval between a pair of probes 3a and 3b when viewed along the extending direction of the transparent electrodes 11a. The dummy conductors 11g(1) are separated parallel to each other by gaps 11v (where conductors are not formed) which extend in the extending direction of the transparent electrodes 11a, and thus constitutes a stripe form. The dummy conductors 11g(2), on the other hand, are mutually separated by gaps 11h (where conductors are not formed) extending in the array direction of the transparent electrodes 11a in a pitch shorter than

the prescribed interval between the probes 3a and 3b when viewed along the extending direction of the transparent electrodes 11a.

When a test is performed as to whether each set of two mutually-adjacent transparent electrodes 11a suffer a short-circuit problem by moving the probes 3a and 3b to the right as viewed in Fig. 1, the dummy pattern 11G having the dummy conductors 11g(1) and the dummy conductors 11g(2) as described above ensures that the probes 3a and 3b, even when moved from the display driving area E into the non-driving area F, avoid the conventionally-suffered problem of, as shown in Fig. 6, simultaneously contacting on a single dummy conductor 11g, and instead contact respectively on distinct one of two dummy conductors 11g without fail. Thus, no short-circuit between the probes 3a and 3b results from the dummy conductors 11g.

Fig. 2 is a schematic diagram illustrating advantages of a dummy pattern according to this embodiment, in which G_t and G_p indicate the intervals between the probe 3a and the probe 3b respectively in the extending direction and in the array direction of the transparent electrodes 11a. Referring to Fig. 2, the tester 3 moves the probes 3a and 3b from the display driving area E to the non-driving area F in the array direction of the transparent electrodes 11a (to the right in Fig. 2). The dummy conductors 11g(2-1) are

mutually set apart by a gap 11h between the probe 3a and the probe 3b at least in the extending direction of the transparent electrodes 11a. Thus, the probe 3a and the probe 3b are not allowed to simultaneously contact on a single dummy conductor 11g, and thereby short circuits resulting from the dummy pattern 11G are eliminated.

The above structure is only workable, however, as long as the gap 11h separating the dummy conductors 11g(2-1) is so placed that the probes 3a and 3b are moved thereover. Accordingly, the structure requires that the scanning position of the tester 3 be set across the gap 11h, thus diminishing the flexibility of the testing position.

The above problem may be avoided, as in the embodiment shown in Fig. 1, by separating the dummy conductors 11g(2-1) by the gaps 11h having a pitch shorter than G_t when viewed along the extending direction of the transparent electrodes 11a, so that the dummy conductors 11g(2-2) are formed. This ensures, regardless of the scanning position of the tester 3 relative to the gaps 11h, that the probe 3a and the probe 3b are always mutually across one of the gaps 11h, thus preventing for sure short circuits resulting from the dummy pattern 11G.

Fig. 3 is another schematic diagram illustrating advantages of this embodiment. Referring to Fig. 3, the dummy conductors 11g(1) and the gaps 11v therebetween

constituting the dummy pattern 11G are formed in the same pitch as that of the transparent electrodes 11a when viewed along the array direction of the transparent electrodes 11a. (G_p is set equal to the above pitch.) Thus, the probes 3a and 3b can be continuously moved from the display driving area E to the non-driving area F without causing short circuits resulting from the dummy pattern 11G.

In the above example, particularly by forming the dummy conductors 11g to be in phase with the transparent electrodes 11a along the array direction of the transparent electrodes, erroneous detection can be prevented for sure without altering the operation cycle of the probes 3a and 3b in the course of an inspection.

The dummy pattern 11G shown in Fig. 1 includes both the dummy conductors 11g(1) and the dummy conductors 11g(2). This allows for more flexibility in probe operations while preventing erroneous detection, and more tolerance for different probe intervals.

It is to be understood that an inspection method and an electro-optical device according to the present invention are not restricted by the above-described examples and that various modifications may be made without departing from the gist of the present invention. For example, the structure of conductor pattern and dummy pattern as described above may be implemented as an electrode pattern and a wiring

pattern formed on the transparent substrate 12 as well as on the transparent substrate 11. Furthermore, the object to be inspected may be wiring lines instead of the electrodes described above, and the inspection method may be applied to any type of conductive members.

Accordingly, the present invention, in which dummy conductors disposed in the array direction of conductors are formed in segments so as to prevent any two or more of test probes from contacting on one of the dummy conductors simultaneously, and to serves to prevent short circuits between any of the probes resulting from the dummy pattern when the probes are progressively moved in the array direction of conductors for inspection, thereby avoiding erroneous detection and achieving quick and simple determination from the test results as to whether the conductor pattern is defective or not.

CLAIMS

What is Claimed is:

1. A conductor-pattern testing method for inspecting an electrode substrate having a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each other on a base and further having a dummy pattern constituted by a plurality of dummy conductors formed in an area on said base where said conductor pattern is not formed, said method examining electrical characteristics among said plurality of conductors by establishing the contact of at least two probes having a positional relationship defined so that the two probes are brought into contact with at least two conductors among said plurality of conductors,

wherein said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern are formed in segments so as to prevent two or more of the probes from being simultaneously in contact with any one of said plurality of dummy conductors and said at least two probes are progressively moved for inspection in the array direction of said plurality of conductors.

2. A conductor-pattern testing method according to Claim 1, wherein said plurality of conductors are electrodes or wiring lines formed on said base.

3. A conductor-pattern testing method according to Claim 1, wherein said dummy conductors disposed in the array direction of said plurality of electrodes to constitute said dummy pattern are mutually set apart between any pair of said at least two probes in the extending direction of said plurality of electrodes.

4. A conductor-pattern testing method according to Claim 1, wherein each of said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern is shorter when viewed along the extending direction of said plurality of conductors than the minimum length between any pair of said at least two probes in the extending direction of said plurality of conductors.

5. A conductor-pattern testing method according to Claim 1, wherein said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern are mutually separated in the array direction of said plurality of conductors.

6. A conductor-pattern testing method according to Claim 1, wherein said base is a substrate, and said electrode substrate is an electro-optical device in which a plurality of electrodes and wiring lines are formed in a particular pattern on the surface of said substrate and electro-optical material to be affected by an electric field generated by said plurality of electrodes are further disposed thereover.

7. An electro-optical device having a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each other on a base, further having a dummy pattern constituted by a plurality of dummy conductors formed in an area on said base where said conductor pattern is not formed, and in which electro-optical material is disposed on said conductor pattern, wherein said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern are mutually separated in the extending direction of said plurality of conductors.

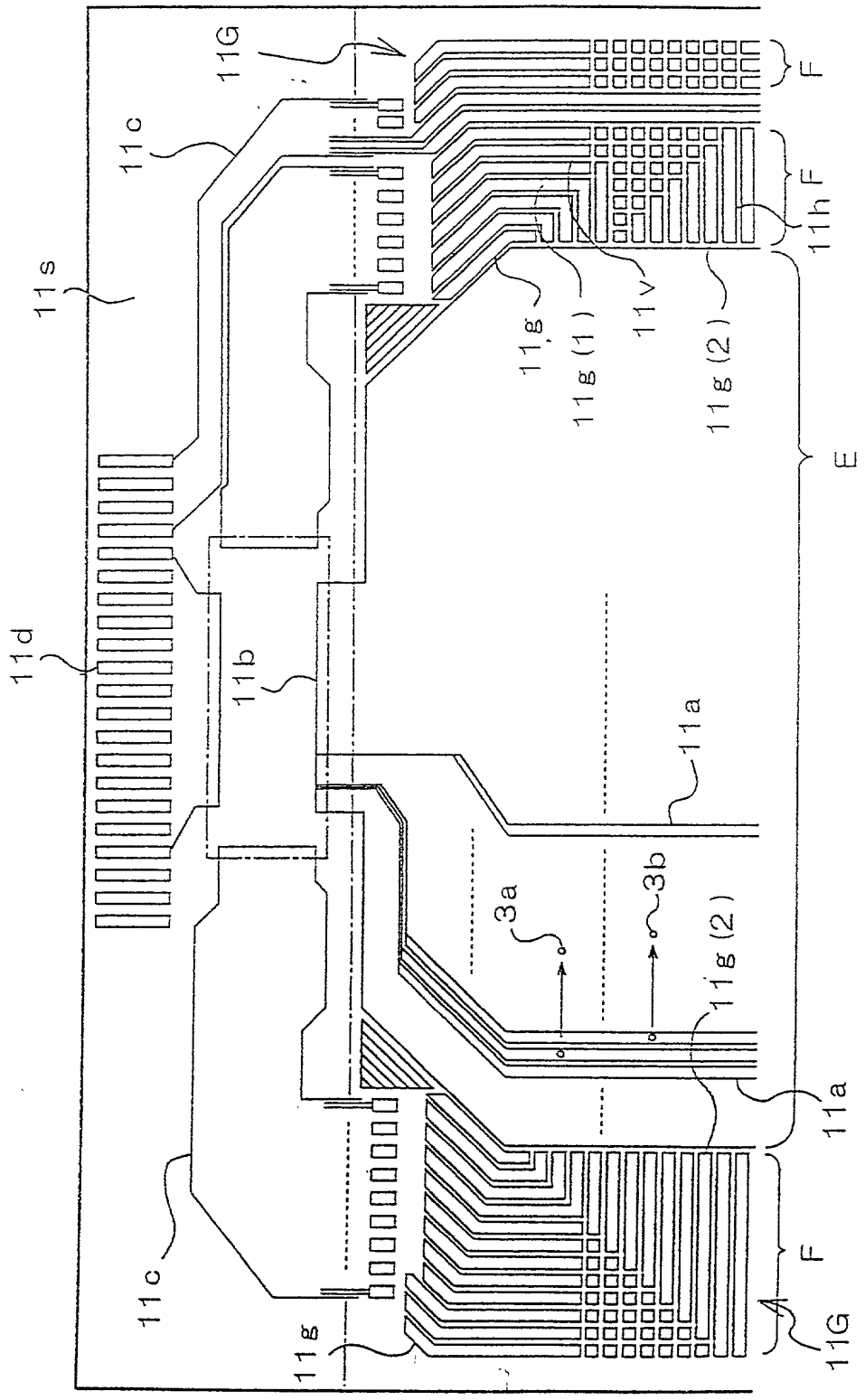
8. An electro-optical device having a conductor pattern constituted by a plurality of elongated conductors formed in parallel to each other on a base, further having a dummy pattern constituted by a plurality of dummy conductors formed in an area on said base where said conductor pattern is not formed, and in which electro-optical material is disposed on said conductor pattern, wherein said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern are mutually separated in the array direction of said plurality of conductors.

9. An electro-optical device according to Claim 8, wherein said plurality of dummy conductors disposed in the array direction of said plurality of conductors to constitute said dummy pattern are mutually separated in the extending direction of said plurality of conductors.

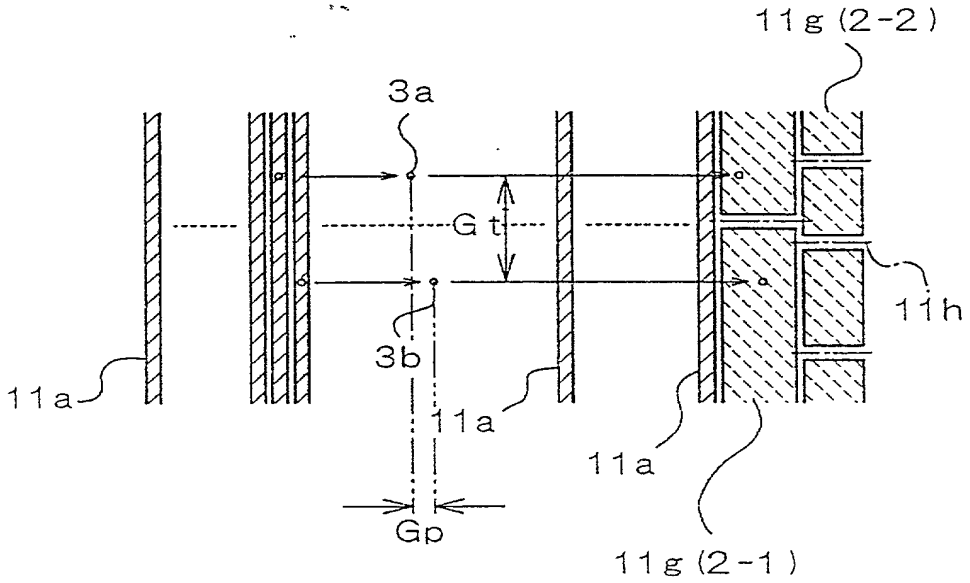
ABSTRACT

A dummy pattern 11G is so configured that each of dummy conductors 11g are mutually set apart with a spacing as appropriate in the extending direction (top-and-bottom direction) and in the array direction (right-and-left direction) of the transparent electrodes 11a.

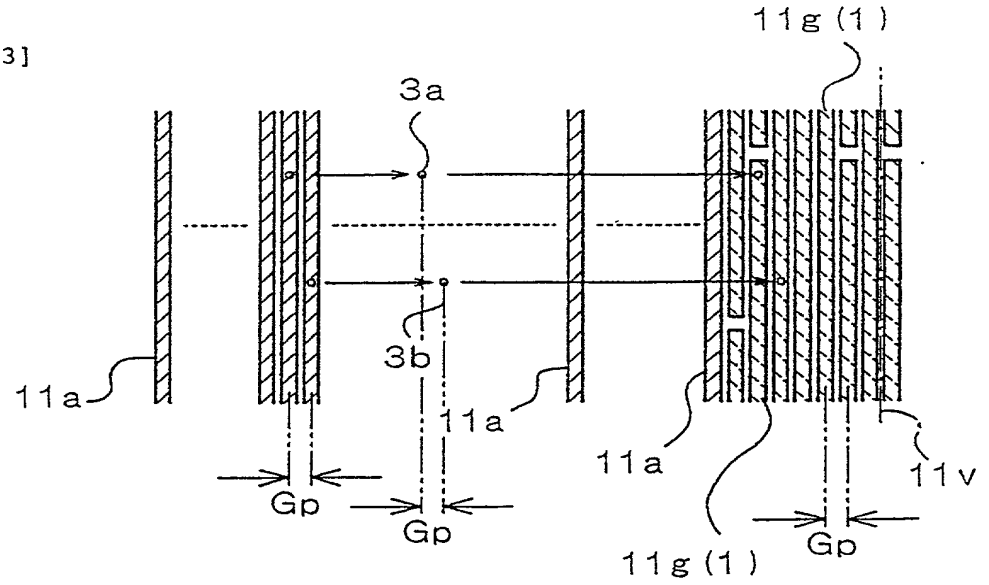
[FIG. 1]



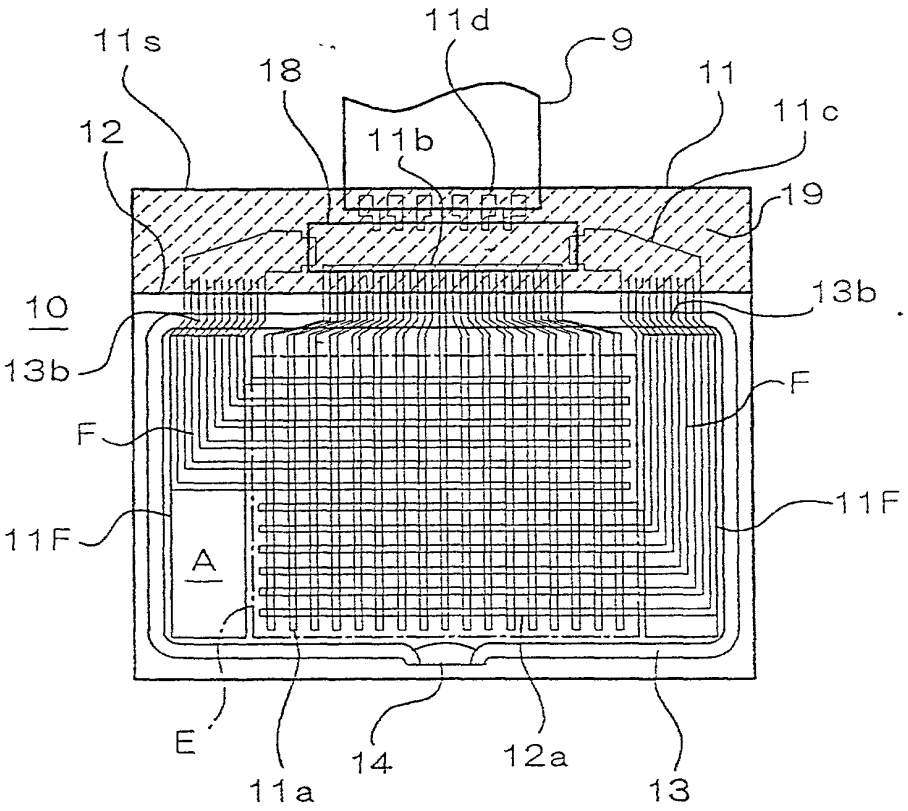
[FIG. 2]


11g (2-2)
3a
Gt
11h
3b
11a
11a
11a
Gp
11g (2-1)

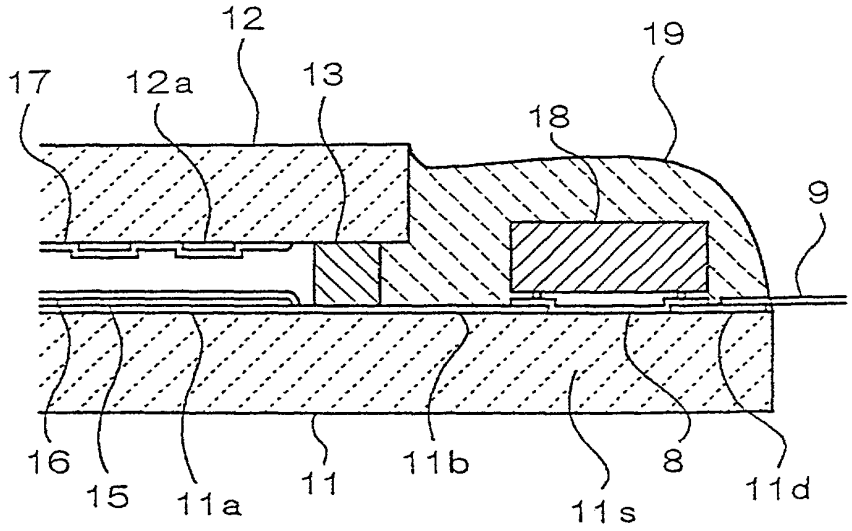
[FIG. 3]


11g (1)
3a
3b
11a
11a
11a
11v
Gp
Gp
Gp
11g (1)

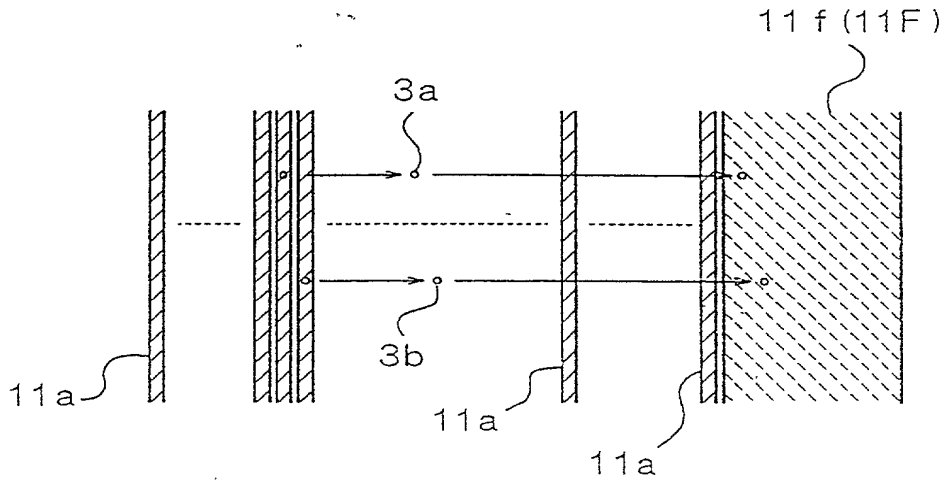
[FIG. 4]


11s
18
11d
9
11
11c
12
11b
19
13b
10
13b
F
F
11F
11F
A
E
11a
14
12a
13

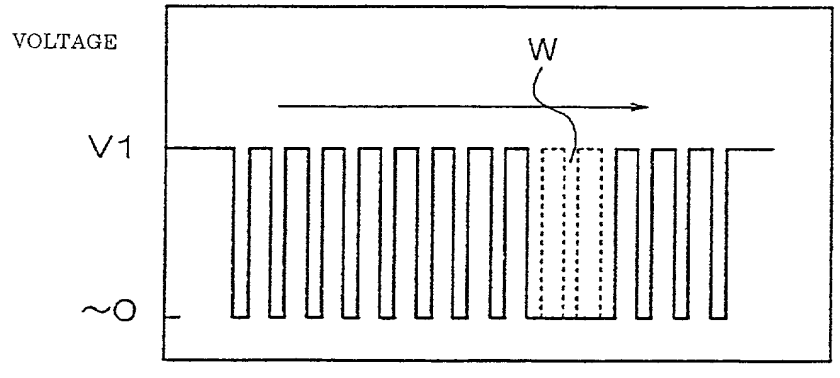
[FIG. 5]


12
19
17
12a
13
18
9
16
15
11a
11
11b
11s
8
11d

[FIG. 6]


11f(11F)
3a
3b
11a
11a
11a

[FIG. 7]


VOLTAGE
W
V1
~0
TIME (NUMBER OF ELECTRODES OR WIRING LINES)

[FIG. 8]